

INFORMATION ABOUT RESEARCH RESULTS

Dissertation title : A three-level boost T-type inverter under normal and failure of semiconductor device modes.

Major : Electronic Engineering Major code: NCS2020

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1. Dissertation summary

A PWM technique for a 3-level boost T-type inverter (3L-qSBT²I) is proposed. The proposed technique not only reduces the current ripple of the boost inductor, but also increases the voltage gain and high modulation index. In addition, the proposed PWM technique also reduces the voltage stress on the component as well as reduces the total harmonic distortion (THD).

Inverter stability and reliability are important in power distribution systems such as: uninterruptible power supply systems, high power medical systems and grid-connected energy conversion systems. For these reasons, the author proposed a PWM technique to the 3-level boost T-type inverter configuration with fault tolerance when the semiconductor power switches are open-circuited (FT-3L-qSBT²I). The technique not only improves the control parameters, but can also operate under fault conditions of the power transistors. In addition, the author proposes a control method to reconfigure the 3-level T-type inverter when open-circuit fault occurs at switches of impedance-source network.

During operation, the inverter generates a common mode voltage (CMV), the CMV is the main cause of many problems for the inverter such as: leakage current, shaft voltage in motor control applications as well as electromagnetic interference. To overcome this disadvantage a common mode voltage reduction technique is proposed. With the modified space vector modulation technique, the method not only suppresses the common mode voltage, but also improves the voltage gain of the three-level boost T-type inverter.

In addition, the authors have used PSIM software and built a experimental prototype to verify the operation of a three-level quasi-switched boost T-type inverter with fault tolerance and common mode voltage reduction methods.

In this thesis, the author make 3 proposals: 1) PWM technique for 3-level quasi-switched boost T-type inverter, 2) reconfiguration method for 3-level boost T-type inverter when the semiconductor devices are open-circuit, and 3) space vector modulation techniques for a three-level boost T-type inverter to reduce common mode voltage. This is not only a new scientific contribution, but also has the potential to master the technology of the future.

2. Contributions of the thesis

The proposed space vector modulation for a 3-level boost T-type inverter configuration can improve the performance of the inverter and enhance the stability of the system. In addition, the effects of common-mode voltage are also limited by the proposed method. From there, it is possible to expand the applications of the inverter in grid-connected systems, photovoltaic cells, ...

HCMC, 25/07/2023

PhD candidate

(Sign and name)

A handwritten signature in blue ink, appearing to read 'Thanh', with a horizontal line underneath it.

Trần Vĩnh Thanh